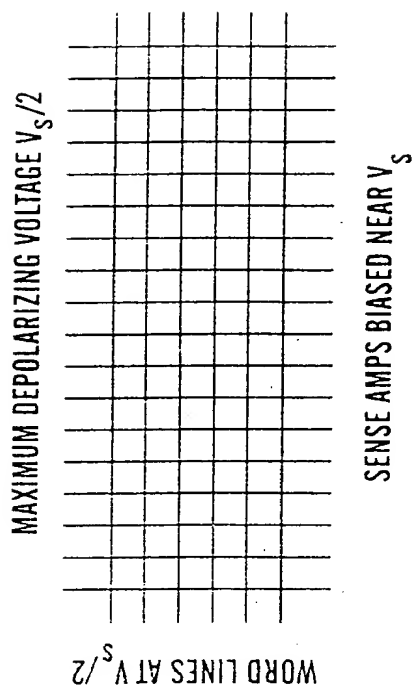




Approved
6/2/03
JMT

- t_0 : WORD LINE LATCHED, ACTIVE PULLED DOWN TO 0
- t_1 : BIT LINE CLAMP RELEASED - SENSE AMP ON
- t_2 : BIT LINE DECISION - DATA LATCHED
- t_3 : WORD LINE RETURNED TO QUIESCENT $V_S/2$
- t_4 : WRITE DATA LATCHED ON BIT LINES
- t_5 : WORD LINE PULLED TO V_S - SET/RESET CAPS ~~CELL~~
- t_6 : WORD LINE RETURNED TO QUIESCENT $V_S/2$
- t_7 : BIT LINES ACTIVELY RETURNED TO V_S CLAMP
- t_8 : READ/WRITE CYCLE COMPLETE



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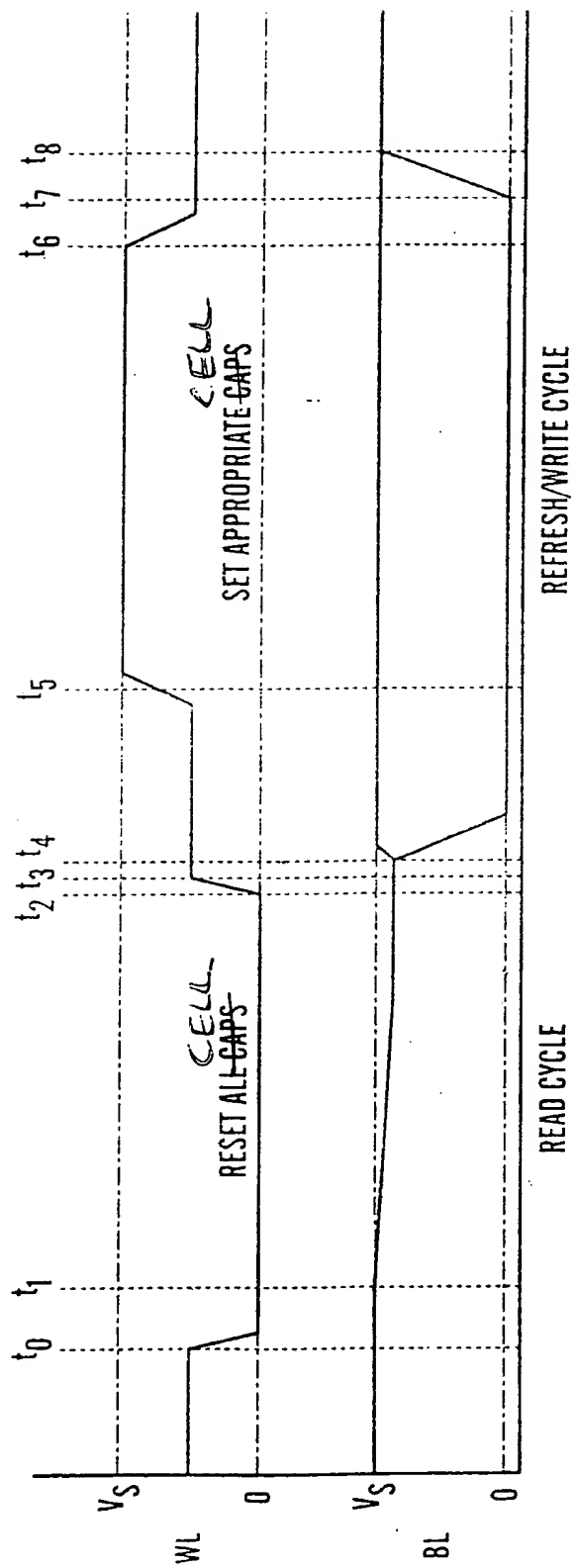


Fig. 4

Approved
6/2/03
Jdd

- t_0 : WORD LINE LATCHED, ACTIVE PULL UP TO V_s
- t_1 : BIT LINE CLAMP RELEASED - SENSE AMP ON
- t_2 : BIT LINE DECISION - DATA LATCHED
- t_3 : WORD LINE RETURNED TO QUIESCENT $V_{s/2}$
- t_4 : WRITE DATA LATCHED ON BIT LINES
- t_5 : WORD LINE PULLED TO 0 - SET/RESET GAPS *CELL*
- t_6 : WORD LINE RETURNED TO QUIESCENT $V_{s/2}$
- t_7 : BIT LINES ACTIVELY RETURNED TO 0 CLAMP
- t_8 : READ/WRITE CYCLE COMPLETE

WORD LINES AT $V_{s/2}$

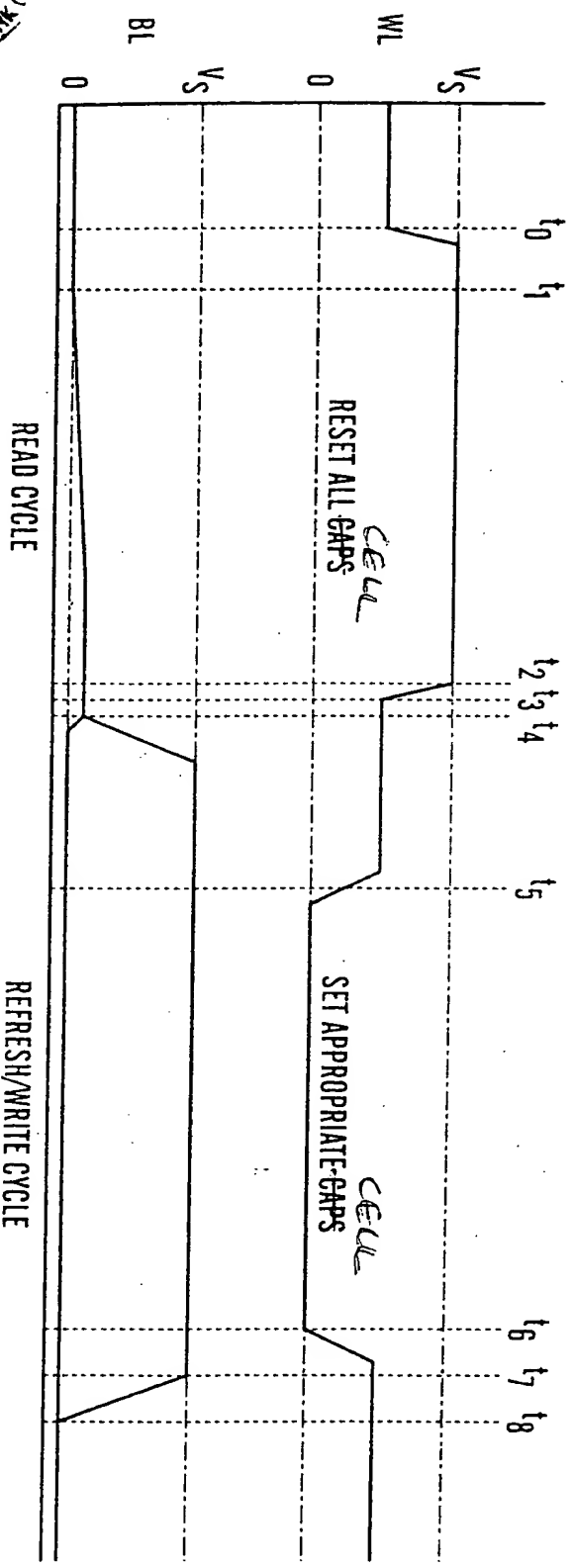
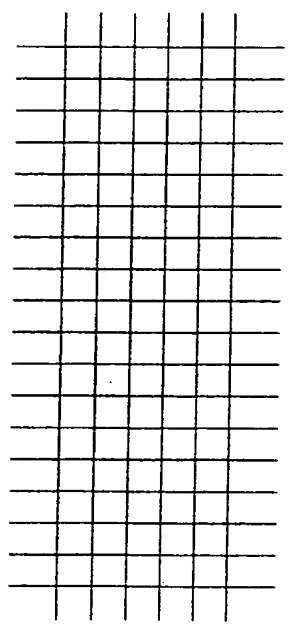


Fig.5